

Start-Up Considerations for 56F8300 and 56F8100 Family Devices

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1. Introduction

The 56F8300 and 56F8100 families of devices contain a number of features designed to ensure reliable start-up from a power-off condition. This application note provides the background you need to best take advantage of these features.

Issues which must be considered include:

- Oscillator start-up times
- Reset timing
- Minimum voltage requirements for high speed
- Supply ramp times

Note: For brevity and clarity, when referring to both the 56F8300 and 56F8100 versions of a device or device family, the term “56F8xxx” will be used. For example, “56F8x2x” refers to both 56F832x and 56F812x devices.

2. Oscillator Start-up

56F8300 and 56F8100 devices fall into two categories with respect to clock generation. The 56F832x devices boot from an internal relaxation oscillator. The relaxation oscillator’s start-up time is negligible, and can be ignored.

The 56F8x4x, 56F8x5x and 56F8x6x devices boot from an on-chip oscillator which is designed to work with either an external crystal or an external ceramic resonator¹. The oscillator has two power modes: low and high, and boots in the high mode. Use of the high power mode at start-up ensures that

1. A recommended circuit is included in the device’s data sheet.

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oscillations begin reliably, regardless of whether a crystal or resonator is connected to the oscillator pins. Systems which utilize crystals connected to these pins must switch the oscillator mode to low power immediately upon exiting reset. Failure to do so could result in long-term damage to the crystal.

Figure 2-1 and **Figure 2-2** illustrate V_{DD} and the XTAL signal from the oscillator during the power-up sequence. Note that systems utilizing ceramic resonators begin oscillating much faster than those utilizing crystals. However, crystals tend to provide for tighter control over the oscillation frequency.

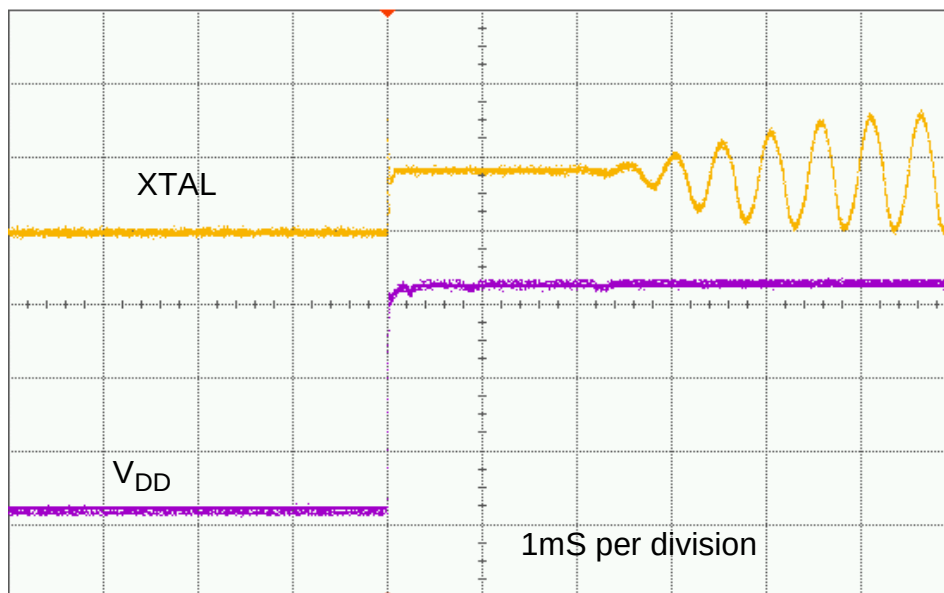


Figure 2-1. Oscillator with Crystal Start-Up Over Time
(the XTAL trace is badly aliased at 1mS per division; the actual oscillation is at 8MHz)

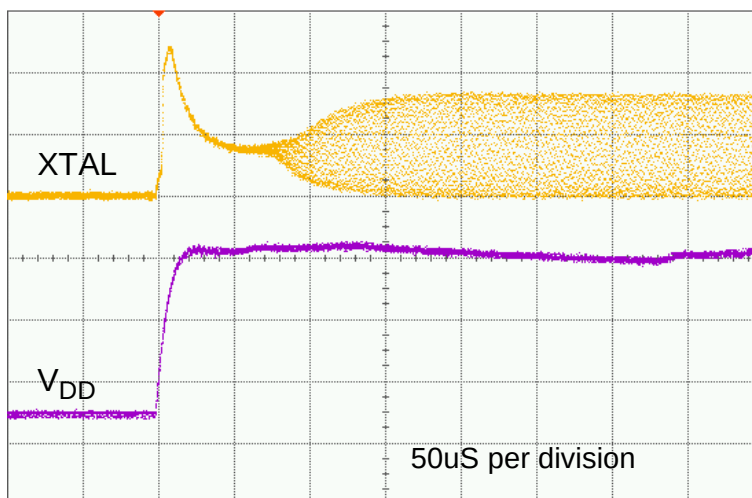


Figure 2-2. Oscillator with Resonator Start-Up Over Time

3. Reset Timing

The power supervisor for the 56F8300 and 56F8100 families include sensors which trigger at the following voltages:

- 1.8V POR¹ on the core logic supply
- 2.2V LVI² on the core logic supply
- 2.7V LVI on the IO supply

The core logic supply must be within the range of 2.25 to 2.75 for normal operation, and the IO supply must be 3.0 to 3.6V for normal operation. It is assumed that the core supply rises in lockstep with the IO supply. This happens naturally when using the internal core regulator. Deriving the 2.5V rail from the 3.3V rail externally should also work.³

The 56F8300 and 56F8100 families of devices give the designer the choice of relying on the internal power supervisor circuit, or providing an external signal to reset the part. When using the internal power supervisor to reset the device, the external $\overline{\text{RESET}}$ pin should be tied resistively to V_{DD} . Operation of the 56F8x2x devices is different from the other devices in the family. Both configurations are discussed in the following sections.

1. POR = Power-On Reset

2. LVI = Low-Voltage Interrupt

3. For all but the 56F8x22, which do not support the option of an external regulator

3.1 POR in the 56F8x2x

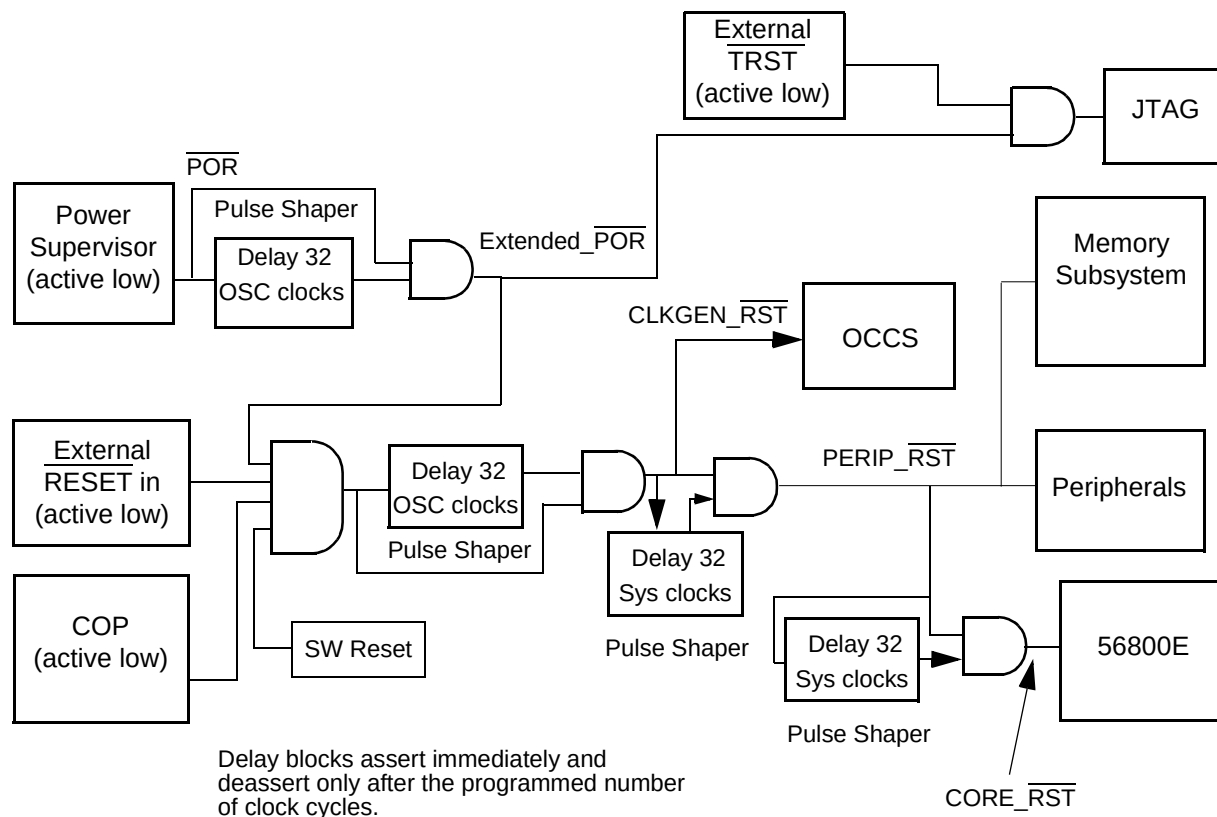


Figure 3-1. 56F8x2x Sources of System Reset

Figure 3-1 is a block diagram illustrating the various sources of system reset for the 56F8x2x devices. Note how release of the reset signal is phased sequentially through the clock generation circuit, peripheral set, and, finally, the core. The $\overline{POR}$ signal from the power supervisor is released only after the POR and both LVI sensors have cleared. It does not assert again until the core logic supply drops below approximately 1.8V. This ensures that the core is released from reset only after the supplies have ramped to acceptable levels, while taking advantage of the low voltage interrupts to give the system sufficient time to shut down in a controlled manner during power down.

3.2 POR in the 56F8x4x, 56F8x5x and 56F8x6x

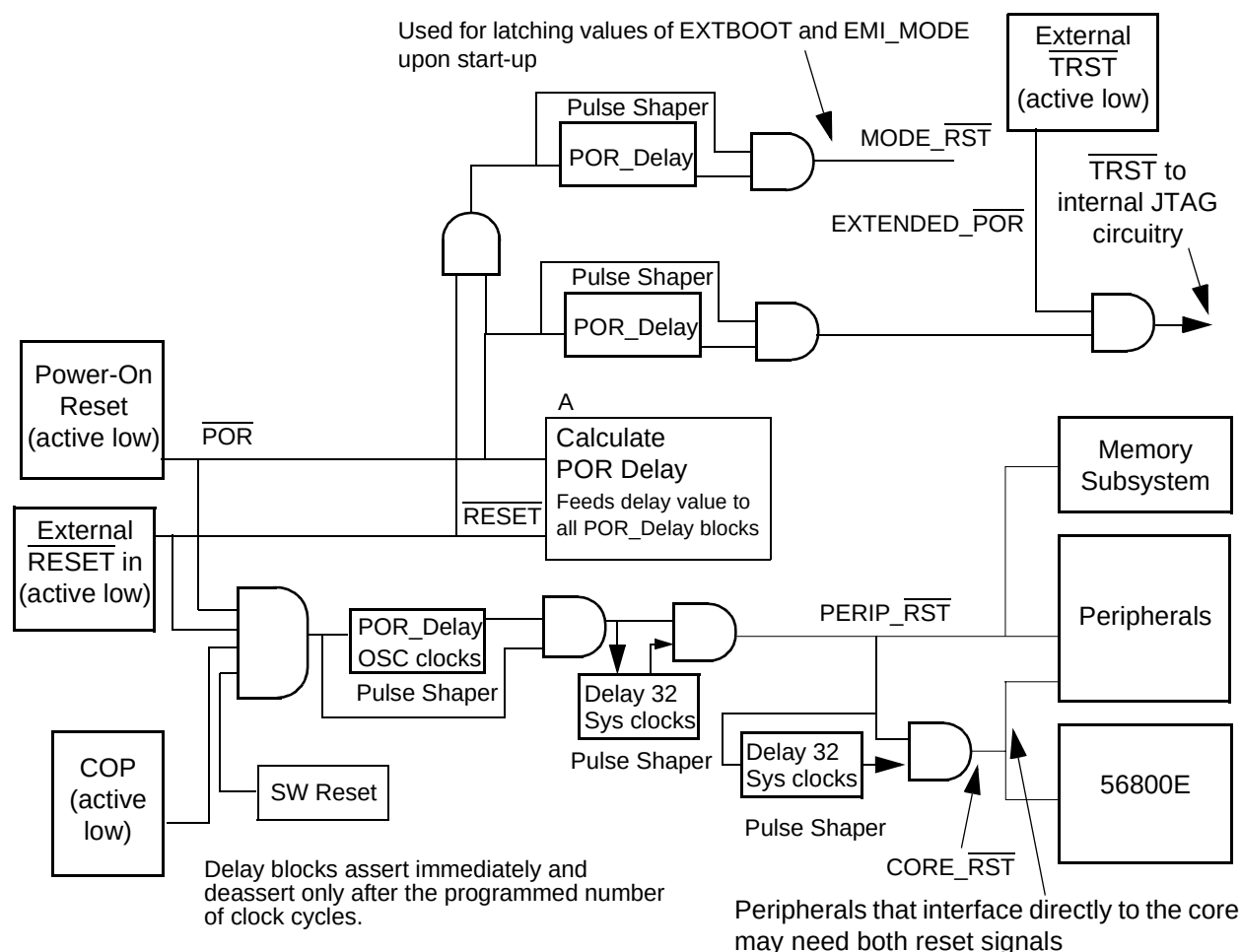


Figure 3-2. 56F8x4x, 56F8x5x & 56F8x6x Sources of System Reset

Figure 3-2 illustrates reset circuitry for the remaining members of the 56F8300 and 56F8100 families. In this case, the $\overline{\text{POR}}$ signal is dependent only upon the 1.8V core supply sensor. If $\overline{\text{RESET}}$ is a logic zero upon power-up, then it is assumed that an external power supervisor is controlling the process, and the POR_Delay is set to 32 clock cycles. If $\overline{\text{RESET}}$ is high, then it is assumed that the internal circuit is responsible for delaying deassertion of reset by a period long enough for supplies to hit their nominal operating range. In this case, POR_Delay is set to 2^{21} clock cycles. Assuming an 8MHz clock cycle, that works out to a little over 1/4 second.

If an external power supervisor is used, it must delay deassertion of reset for a period equaling the sum of the supply ramp-up time plus oscillator start-up time. The oscillator start-up time is specified in the device data sheet, and is different for ceramic resonators versus crystals.

4. Minimum Voltage Requirements

Freescale recommends that application start-up code, which normally occurs before *main()*, requires that both low-voltage interrupts have cleared prior to enabling the Phase Locked Loop (PLL) and proceeding into main application. The start-up code should oversample the LVI bits several times to eliminate any effects of system noise. The LVI check is somewhat redundant, as the conditions put forth in the prior sections usually ensure that core and IO voltages have reached legal limits prior to releasing the 56800E core to begin operation, but it does provide an extra degree of safety.

Finally, make sure that both PLL lock bits indicate that the PLL has locked onto the desired frequency prior to switching the system clock source to use the PLL output. Switching to the PLL output prior to achieving lock will result in inconsistent, and probably incorrect, operation over time and between multiple devices.

5. Troubleshooting

If you encounter start-up problems, check the following:

1. Confirm 3.3V is present on V_{DD_IO} and $V_{DDA_OSC_PLL}$ and V_{DDA_ADC}
2. Confirm 2.5V is present on the V_{CAP} pins
3. How long are the ramp rates for the supply pins?
4. If using an external power supervisor, did $\overline{RESET}$ deassert, and how long was it asserted?
5. If using the internal power supervisor, was $\overline{RESET}$ high during the power-up sequence?
6. If using a crystal or resonator, are the XTAL and EXTAL pins oscillating?
7. Does your oscillator circuit match that suggested in the device data sheet?
8. If using an external clock source, is the clock signal present on XTAL and is EXTAL grounded?
9. If using an external power supervisor, was $\overline{RESET}$ asserted until after the oscillator was operating?
10. Does the $\overline{RSTO}$ signal deassert on devices in which it is pinned out? This signal represents the reset state of the 56800E. It should take approximately 1/4 second to deassert when using the internal power supervisor. It should deassert less than 1.5 μ sec (assuming an 8MHz clock source) after an external power supervisor deasserts.
11. Modify your pre-*main()* startup code to enable the CLK0 pin for devices in which it is present, then monitor this pin to ensure your internal clocks are active
12. Try updating your Metrowerks stationery. A corrupted start-up routine can make a part appear to be inoperative when, in fact, there is a software issue.
13. For all but the 56F8x22 devices, is the OCR_DIS pin set to ground when utilizing the internal core logic regulator? Set to V_{DD_IO} when utilizing an external regulator?
14. For the 56F8x4x, 56F8x5x and 56F8x6x devices, is the CLKMODE pin set to ground for devices using an external resonator or crystal? Set to V_{DD_IO} when using an external clock source?

15. For the 56F8x2x devices, did things go astray after switching to an external resonator or crystal? If so, ensure that internal pull-ups are still disabled via GPIO_C_PUR[1:0]. Are the XTAL and EXTAL pins still programmed for use by the oscillator and not by the GPIO in GPIO_C_PER[1:0]? Is the CLKMODE bit in the OSCTL set to Logic zero? (It defaults to one.)
16. If you have the ability to monitor the supply currents, do they match expected values? See the application note “**Controlling Power Consumption**”, AN1991, for expected values.
17. Do you have at least 4.4μF (total) of capacitance or more on the V_{CAP} pins when using the internal regulator? If not, the internal supply could droop when switching to a high core frequency. Monitor the V_{CAP} pins with your scope.
18. For devices which have EXTBOOT and EMI_MODE pins, are they set to the correct values?
19. If booting from external memory, do you see address bus activity?
20. Contact Freescale Technical Support for assistance:
<http://www.freescale.com>

6. Conclusions

The 56F8300 and 56F8100 devices are designed to be robust, and should start reliably. By observing the simple suggestions given in [Section 2.](#) through [Section 4.](#), you should be able to avoid any problems with your application. And if you do have problems, the troubleshooting procedure outlined in [Section 5.](#) will allow you to quickly spot and correct the problem.

7. References

The following references can be found on the Freescale web site at:

<http://www.freescale.com>

1. *56F8300 Peripheral User Manual*, MC56F8300UM
2. *56F83xx/56F81xx Technical Data* document specific to the device you’re implementing
3. *DSP56800E Reference Manual*, DSP56800ERM

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